REMARKS

Claims 1-34 are pending, with claims 1, 8, 11, 16, 21, 25 and 33 being independent. Claims 1-10 have been canceled without prejudice. Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim Objections

Claim 26 stands objected to because, "in the final line, perhaps the word 'affect' is more appropriate than 'effect'". First, it is noted that claim 26 does not include the word "effect". Second, assuming that claim 21 is the claim to which the objection refers (claim 21 includes "effect" in the last line), the word choice here is correct. The verb "affect" means to produce a change in something, whereas the verb "effect" means to produce or bring about something. Thus, the claim objection is traversed, and no change in the claim language is required.

Interview Summary

Examiner Johnson is thanked for the interview, which was conducted with Mr. Hunter on November 30, 2006. During the interview, claims 11 and 16, and paragraphs 54 and 55 of the

09/21/2006 Office Action were discussed. The arguments presented were: (1) while it is true that locks are not required for synchronization generally, acquiring a lock is required by claims 11 and 16, and the statements regarding "Applicant's invention" in paragraph 54 of the 09/21/2006 Office Action are inaccurate; and (2) the statement in paragraph 55 of the 09/21/2006 Office Action that, "Rajwar speculatively executes a critical section (or, in other words, speculatively avoids a read-modify-write lock)" (emphasis added) is correct and clearly shows the difference between Rajwar and the presently claimed subject matter.

Regarding point (1) above, Agreement was reached that Examiner Johnson did not fully understand the claimed subject matter at the time the 09/21/2006 Office Action was issued, and Examiner Johnson requested further explanation of the differences between Rajwar and the presently claimed subject matter in this written response. Regarding point (2) above, Examiner Johnson had not familiarized himself enough with the case to be sure how to respond, and thus, no agreement was reached.

Claim Rejections under 35 U.S.C. 102

Claims 11, 12, 15-17, and 20 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Rajwar (Speculative Lock Elision). This contention is respectfully traversed.

Independent claims 11 and 16 each recite, "effecting synchronization between the parallel processes using processor speculation in the data processing machine[.]" Thus, processor speculation is used to bring about synchronization between the parallel processes. In stark contrast, Rajwar describes systems and techniques for avciding synchronization altogether.

The Office states that the "use of lock speculation is not avoiding synchronization for a variety of reasons." (*See* OA mailed 09/21/2006 at p. 21, ¶ 54.) Without conceding to the reasons given by the Office, Applicant agrees with this statement, but notes that it is the present application which teaches the use of lock speculation, not Rajwar.

Rajwar describes lock elision (i.e., omission) using speculation. Rajwar explicitly states that, "Synchronization instructions are predicted as being unnecessary and elided. [...] Successful speculative elision is validated and committed without acquiring the lock." (*See* Rajwar at Abstract, page 294, col. 1; emphasis added.) Rajwar dynamically removes the

synchronization locks around critical sections, and then performs critical sections speculatively. The process is summarized by Rajwar as follows:

> In this paper, we show how hardware techniques can be used to remove dynamically unnecessary serialization from an instruction stream and thereby increase concurrent execution. In Speculative Lock Elision (SLE), the hardware dynamically identifies synchronization cperations, predicts them as being unnecessary, and elides them. By removing these operations, the program behaves as if synchronization were not present in the program. Of course, doing so can break the program in situations where synchronization is required for correctness. Such situations are detected using pre-existing cache coherence mechanisms and without executing synchronization operations.

(*See* Rajwar at Section 1, page 295, col. 1; emphasis added.) The Office notes that Rajwar does obtain a lock when the speculation is unsuccessful. (*See* OA mailed 09/21/2006 at p. 21, ¶ 54.) But it should be further noted that Rajwar does not obtain a lock when the speculation is successful, and this is precisely the point of distinction between Rajwar and the presently claimed subject matter.

The Office notes that, in general usage of the term "synchronization", locks are not required for synchronization. (*See* OA mailed 09/21/2006 at p. 21, ¶ 54.) For this reason, claims 11 and 16 were previously amended to clarify the claimed subject matter and recite, "effecting synchronization between the parallel processes using processor speculation in the data processing machine to speculatively read-modify-write a lock variable associated with a critical section[.]" (Emphasis added.) Thus, the synchronization being claimed is clearly limited to the use of speculation to acquire a lock variable used to enforce mutual exclusion for a critical section, and this clearly differentiates the claimed subject matter from Rajwar.

Rajwar's method does not speculatively read-modify-write a lock variable because Rajwar's method is based on not doing a lock variable write when doing speculation. To give a concrete example, suppose two critical sections are guarded by the same lock, but access different data in a given run. In this case, Rajwar would avoid grabbing a lock, avoid synchronization, and allow the two critical sections to be executed in parallel. In contrast, the presently claimed subject matter would grab the lock (using speculation) and not allow the two critical sections

to be executed in parallel. This is why Rajwar teaches avoiding synchronization, whereas the presently claimed subject matter does not. Rather, the presently claimed subject matter seeks to make synchronization more efficient through speculative execution of the lock acquisition code.

The Office accurately describes Rajwar when saying, "Rajwar speculatively executes a critical section (or, in other words, speculatively avoids a read-modify-write lock) and, if mis-predicted, re-executes with the lock." (*See* OA mailed 09/21/2006 at pp. 21-21, ¶ 55.) However, this is not the technique disclosed in Applicant's FIG. 5 (as suggested by the Office) because FIG. 5 clearly shows the "commit" instruction coming before the critical section. Thus, the lock is acquired using speculative execution, and the critical section is not executed without the lock first being acquired, which is in stark contrast with Rajwar.

Thus, for all of the above reasons, independent claims 11 and 16 should be patentable over Rajwar. Dependent claims 12, 15, 17 and 20 should be patentable over Rajwar for at least the above reasons.

Claims 11, 15, 16, and 20 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Transactional Memory (Moss). This contention is respectfully traversed.

The Office notes that Moss teaches "lock-free synchronization", but then further asserts that Moss teaches using processor speculation in a data processing machine "to speculatively read-modify-write a lock variable associated with a critical section". (*See* OA mailed 09/21/2006 at p. 5, ¶ 14.) This contention cannot be maintained.

Lock-free synchronization and using processor speculation in a data processing machine to speculatively read-modify-write a lock variable associated with a critical section are mutually exclusive of each other, by definition. For synchronization to be lock-free, there must be no lock. Moss makes very clear that what is described in Moss is an alternative to using a locking technique. (*See* Moss at p. 289, col. 2.) Thus, Moss does not teach or suggest effecting synchronization between parallel processes using processor speculation in a data processing machine to speculatively read-modify-write a lock variable associated with a critical section.

For at least the above reasons, claims 11, 15, 16, and 20 should be patentable over Moss.

Claims 1, 6, 7, 14 and 19 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Moss in view of Lam (Enhancing Software Reliability with Speculative Threads). Claims 21-25, 27 and 31-34 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Moss in view of Lam in view of Rajwar. Claims 2-5 and 8-10 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Moss/Lam in view of Christie (U.S. 6,009,512). Claims 13 and 18 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Rajwar in view of "common prior art". Claim 28 stands rejected under 35 U.S.C. 103() as allegedly being unpatentable over Moss/Lam/Rajwar in view of "common prior art". Claim 26 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Moss/Lam/Rajwar in view of Rajwar. Claims 29 and 30 stand rejected under 35 U.S.C. 103() as allegedly being unpatentable over Moss/Lam/Rajwar in view of "common prior art". These contentions are respectfully traversed.

The rejection of claim 1-10 has been obviated by the cancellation of these claims without prejudice.

Claims 13 and 14 depend from independent claim 11, and claims 18 and 19 depend from independent claim 16. For the reason discussed above, neither Moss nor Rajwar teach or suggest

the subject matter of either claim 11 or claim 16. Neither Christie nor Lam cure the deficiencies of Rajwar and Moss. In particular, it is noted that Lam never describes mutually excluding processes from accessing the same data at the same time. Thus, even if Lam could be combined with Rajwar and/or Moss (which is not conceded), such combinations would not result effecting synchronization between parallel processes using processor speculation in a data processing machine to speculatively read-modify-write a lock variable associated with a critical section.

Thus, for at least the above reasons, claims 13, 14, 18, and 19 should be in condition for allowance.

Furthermore, independent claim 21 recites, "speculatively executing machine instructions, including a memory access instruction, in a processing system to effect synchronization between parallel processes, wherein the speculatively executing comprises performing a speculative read-modify-write to a lock variable associated with a critical section; retiring the speculatively executed machine instructions; and maintaining cache coherence in the processing system during said executing and said retiring to identify a mis-speculation to effect the synchronization between the parallel processes." (Emphasis

added.) Thus, for at least the above reasons, independent claim 21 and its dependent claims 22-24 should be in condition for allowance.

Independent claim 25 recites, "a processor having a processor architecture that provides speculative execution of machine instructions and exposes said speculative execution to program control through at least one machine instruction; and a memory coupled with the processor, the memory embodying information indicative of instructions, including the at least one machine instruction, that result in synchronization between parallel processes when performed by the processor with detection of mis-speculation; wherein performance of the instructions by the processor comprises performing a speculative read-modify-write to a lock variable associated with a critical section." (Emphasis added.) Thus, for at least the above reasons, independent claim 25 and its dependent claims 26-32 should be in condition for allowance.

Independent claim 33 recites, "processing means for speculatively executing machine instructions in response to a speculative execution instruction, including means for detecting a mis-speculation; means for treating multiple speculative instructions as a group for purposes of retirement such that the

multiple speculative instructions are flushed from the processing means together and execution proceeds from an address in response to a detected mis-speculation to effect synchronization between parallel processes; wherein performance of the instructions by the processing means comprises performing a speculative read-modify-write to a lock variable associated with a critical section." (Emphasis added.) Thus, for at least the above reasons, independent claim 33 and its dependent claim 34 should be in condition for allowance.

## Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

It is respectfully suggested for all of these reasons, that the current rejections are overcome, that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

No fees are believed due with this response. Please apply any necessary charges or credits to deposit account 06-1050.

Respectfully submitted,

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